Second Semester Examination
2017/2018 Academic Session

May / June 2018

EEE 344 – SYSTEM VLSI
[SISTEM VLSI]

Duration : 3 hours
[Masa : 3 jam]

Please ensure that this examination paper consists of **EIGHT (8)** pages and **ONE (1)** page of printed appendices material before you begin the examination.

*[Sila pastikan bahawa kertas peperiksaan ini mengandungi **LAPAN (8)** muka surat dan **SATU (1)** muka surat lampiran yang bercetak sebelum anda memulakan peperiksaan ini.]*

Instructions: This question paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry the same marks.

[***Arahan:*** *Kertas soalan ini mengandungi **EMPAT (4)** soalan. Jawab **SEMUA** soalan. Semua soalan membawa jumlah markah yang sama.]*

In the event of any discrepancies, the English version shall be used.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

1. (a) Calculate the threshold voltage V_{T0} at V_{SB} = 0 for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 4 \times 10^{18}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness t_{ox} = 16 Å, and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}.

Hitung voltan nilai ambang V_{T0} di V_{SB} = 0 untuk sebuah transistor polisilikon MOS saluran n yang mempunyai parameter seperti berikut: ketumpatan pengedopan substrat $N_A = 4 \times 10^{18}$cm^{-3}, ketumpatan pengedopan get polisilikon $N_D = 2 \times 10^{20}$ cm^{-3}, Ketebalan oksida get t_{ox} = 16 Å, dan ketumpatan caj tetap oksida $N_{ox} = 4 \times 10^{10}$ cm^{-2}.

(15 marks/markah)

(b) Figure 1 illustrates a pseudo-nMOS inverter circuit. Given V_{DD}=1.2 V, $V_{T0,n}$=0.58 V, $V_{T0,p}$=–0.56 V, $v_{sat,n}$=124340 m/s , $(W/L)_n$ = 12, $(W/L)_p$ = 3, L_n=L_p=40 nm, $C_{ox,n}$=2.20X10^{-2} F/m^2 , k_n'= 94.3 μA/V^2, k_p'=41 μA/V^2, $E_{C,p}L_p$=1.8 V, $E_{C,n}L_n$=0.4 V.

Rajah 1 menunjukkan sebuah litar penyongsang pseudo-nMOS. Di beri V_{DD}=1.2 V, $V_{T0,n}$=0.58 V, $V_{T0,p}$=–0.56 V, $v_{sat,n}$=124340 m/s , $(W/L)_n$ = 12, $(W/L)_p$ = 3, L_n=L_p=40 nm, $C_{ox,n}$=2.20X10^{-2}F/m^2 , k_n'= 94.3μA/V^2, k_p'=41μA/V^2, $E_{C,p}L_p$=1.8 V, $E_{C,n}L_n$=0.4 V.

Calculate:
Hitungkan:

(i) V_{OL}
V_{OL} (10 marks/markah)

(ii) V_{OH}
V_{OH} (5 marks/markah)

(iii) V_{IL}
V_{IL} (30 marks/markah)

(iv) V_{IH}
V_{IH} (30 marks/markah)

(v) Noise Margins
Jidar Hingar (10 marks/markah)

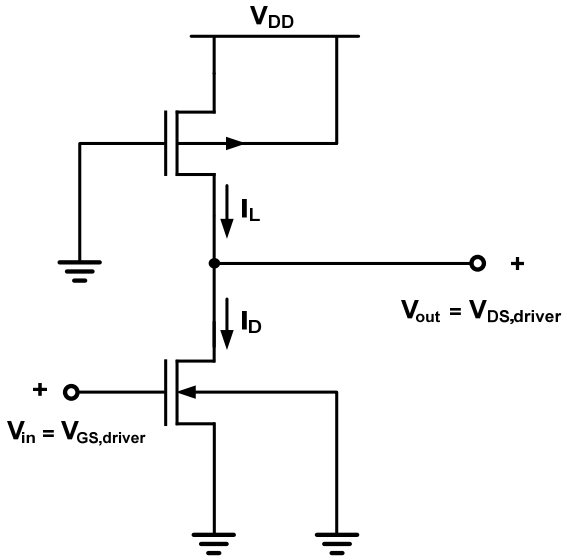

Figure 1
Rajah 1

2. (a) (i) Sketch a three stage ring oscillator consisting of identical inverters.

Lukiskan Oscillator gegelung tiga peringkat yang terdiri daripada penyongsang yang serupa.

(10 marks/markah)

(ii) Express the oscillation period T in terms of average propagation delay.
Nyatakan masa ayunan T dari segi penyebaran masa purata.

(10 marks/markah)

(b) Design a CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors to meet the following specifications:

Rekabentuk sebuah penyongsang CMOS dengan menentukan lebar saluran W_n dan W_p nMOS dan pMOS tersebut untuk memenuhi spesifikasi berikut:

(80 marks/markah)

- V_{th}=0.6 V for V_{DD}=1.2 V
- $\tau_{PHL}^{*} \leq 20$ ps, $\tau_{PLH}^{*} \leq 15$ ps
- A falling delay of 40 ps for an output transition from 0.8 V to 0.1 V
  Masa jatuh 40 ps untuk pertukaran keluaran dari 0.8 V kepada 0.1 V
- A combined output load capacitance of 10 fF
  Gabungan kapasitor bebanan keluaran sebanyak 10 fF

The device parameters are:
Parameter peranti adalah seperti berikut:

- $\mu_n C_{ox}$=184 μA/V^2, $V_{T0,n}$=0.5 V, $E_{c,n}L_n$ = 0.3
- $\mu_p C_{ox}$=46 μA/V^2, $V_{T0,p}$=-0.48 V, $E_{c,p}L_p$ = 1.2
- L=40 nm, W_{min}=300 nm

3. (a) Based on Figure 3(a), the circuit is designed to drive a total capacitive load of C_L = 0.2 pF. For the NMOS device, assume V_{TO} = 1.0 V and k'$_n$ = 50 μA/V^2. For the PMOS devices, assume V_{TO} = -1.0 V and k'$_p$ = 25 μA/V^2. For all the devices, assume the W/L ratios for each transistor is shown in the figure. The initial voltage across the C_L is 0 V. The signal at input *E* is 0 V for all time. For the rest of the input, the signals are shown in the figure.

Berdasarkan Rajah 3(a), litar ini direka untuk memacu C_L = 0.2 pF beban pemuat. Untuk peranti NMOS, andaikan V_{TO} = 1.0 V dan k'$_n$ = 50 μA/V^2. Untuk peranti PMOS, andaikan V_{TO} = -1.0 V dan k'$_p$ = 25 μA/V^2. Untuk semua peranti, andaikan nisbah W/L untuk setiap transistor adalah seperti dalam rajah. Voltan asal bagi C_L ialah 0 V. Isyarat signal dimasukan E ialah 0 V pada setiap masa. Manakala untuk semua isyarat yang lain adalah seperti di dalam rajah.

Calculate the time it takes for voltage across the C_L reaches 50 % of V_{DD}. *Kirakan masa supaya voltan bagi C_L adalah 50 % daripada V_{DD}.*

(40 marks/markah)

(b) Sketch the voltage waveform across the C_L and provide clear marking of 50 % crossing along the time axis.

Lukiskan bentuk gelombang voltan C_L dan dengan jelas tandakan silang 50 % pada paksi masa.

(20 marks/markah)

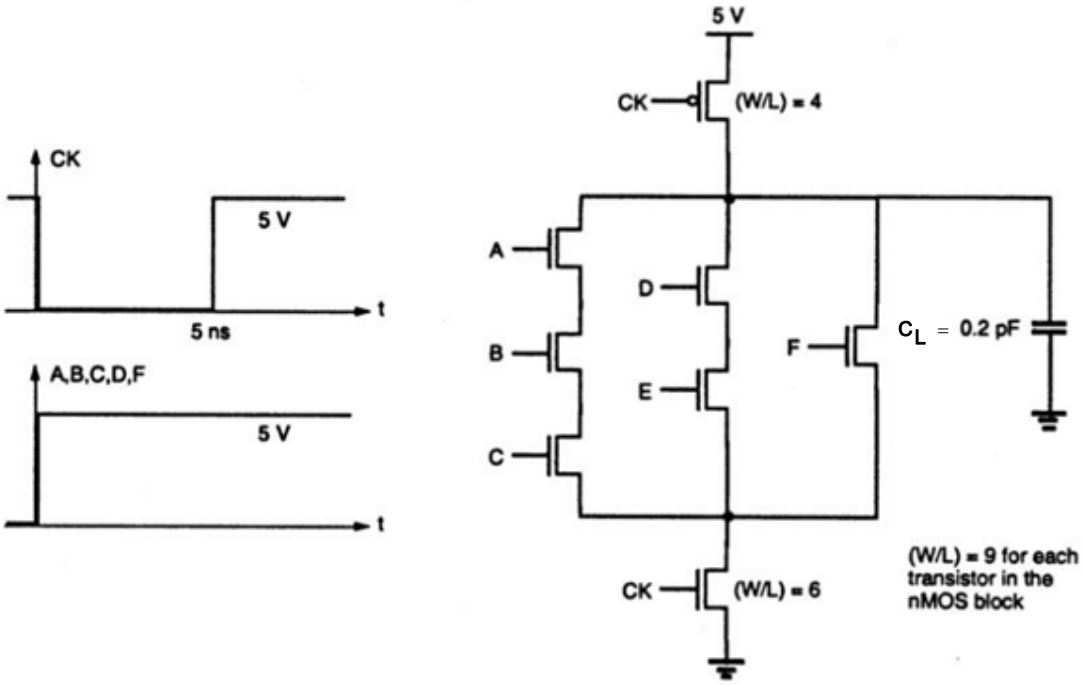

Figure 3(a)
Rajah 3(a)

(c) What is the definition of sequential circuit? Draw a basic CMOS Master-Slave Flip-Flop.

Apakah definisi litar berjujukan? Lukiskan asas Flip-Flop Tuan-Hamba CMOS.

(40 marks/markah)

4. (a) What is volatile memory and non-volatile memory?
Apakah ingatan meruap dan ingatan tak meruap?

(20 marks/markah)

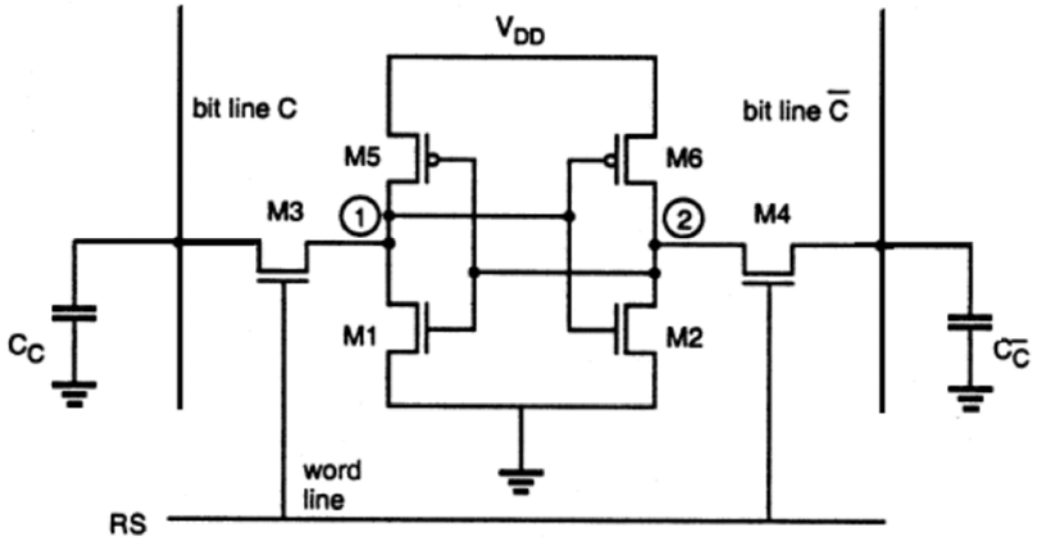

Figure 4(b)
Rajah 4(b)

(b) The circuit in Figure 4(b) has parameters as follows.
Parameter untuk litar dalam Rajah 4(b) adalah seperti berikut.

V_{Ton} = 0.7 V, V_{Top} = -0.7 V, k'n = 20 μA/V2 , k'P = 10 μA/V2 , γ = 0.4 $V^{1/2}$ and |2 φ F| = 0.6 V.

If W/L ratios for M1 and M2 is 1, M3 and M4 is 2/4.
Assuming that the storage bit is 0, state of cell can be changed for $V_C \leq 0.5$ V and M1 initially OFF.

Sekiranya nisbah W/L untuk M1, M2 ialah 1 dan M3, M4 ialah 2/4. Andaikan bit simpanan ialah 0, keadaan sel berubah apabila $V_C \leq 0.5$ V dan pada mulanya M1 TUTUP.

(i) Confirm that M5 is saturated.
Pastikan M5 berada dalam tepu. (15 marks/markah)

(ii) Confirm that M3 is in linear region.
Pastikan M3 berada dalam kawasan lelurus.

(15 marks/markah)

(iii) Determine W/L for M5 and M6.
Tentukan nilai W/L untuk M5 dan M6.

(50 marks/markah)

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APPENDIX
LAMPIRAN

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n R_L} - \sqrt{\left(V_{DD} - V_{T0} + \frac{1}{k_n R_L}\right)^2 - \frac{2V_{DD}}{k_n R_L}}$$

$$\frac{V_{DD} - V_{out}}{R_L} = W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(V_{in} - V_{T0})^2}{(V_{in} - V_{T0}) + E_C L}$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} \frac{1}{\left(1 + \frac{V_{out}}{E_C L_n}\right)} \left[2 \cdot (V_{in} - V_{T0}) \cdot V_{out} - {V_{out}}^2\right]$$

$$V_{OL} = V_{OH} - V_{T0,n} - \sqrt{\left(V_{OH} - V_{T0,n}\right)^2 - \left(\frac{k_p}{k_n}\right) \cdot E_{C,p} \cdot L_p \cdot \frac{\left(V_{DD} - \left|V_{T0,p}\right|\right)^2}{\left(V_{DD} - \left|V_{T0,p}\right|\right) + E_{C,p} L_p}}$$

$$W_n \cdot v_{sat} \cdot C_{ox} \cdot \frac{\left(V_{in} - V_{T0,n}\right)^2}{E_{C,n} L_n}$$

$$\cong \frac{k_p}{2} \cdot \left[2\left(V_{DD} - \left|V_{T0,p}\right|\right) \cdot \left(V_{DD} - V_{out}\right) - \left(V_{DD} - V_{out}\right)^2\right]$$